IN THE CLAIMS

Claim 1 (canceled).

2. (new) A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data and which is separate from said first memory, said processor comprising:

a first terminal for outputting an address for reading at least one graphics data stored in said first memory based on a first clock signal; and

a second terminal for outputting an address for writing graphics data to said second memory based on a second clock signal,

wherein said processor generates graphics data from said read graphics data, and said first and second clock signals are different from each other.

3. (new) A processor according to claim 2, wherein said first memory outputs said graphics data based on said first clock signal.

4. (new) A processor according to claim 2, wherein said second memory outputs said graphics data based on said second clock signal.

5. (new) A processor according to claim 2, wherein said processor, which reads said graphics data from said first memory, generates new graphics data from said read graphics data, and writes said new graphics data to said second memory.

6. (new) A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data for displaying and which is separate from said first memory, said processor comprising:

a first terminal; and

a second terminal,

wherein each terminal outputs an address at a timing different from a timing used to output an address from the other terminal, and

wherein said processor reads graphics data from said first memory based on an address output from said first terminal, generates graphics data for displaying from said read graphics data, and writes said graphics data for displaying to said second memory based on an address output from said second terminal.

7. (new) A processor according to claim 6, wherein said first memory outputs said graphics data based on a first clock signal.

8. (new) A processor according to claim 6, wherein said second memory outputs said graphics data for displaying based on a second clock signal.

9. (new) A processor according to claim 6, wherein said processor, which reads graphics data from said first memory, generates new graphics data from said read graphics data, and writes said new graphics data to said second memory.

10. (new) A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data and which is separate from said first memory, said processor comprising:

a first terminal; and

a second terminal for outputting addresses,

wherein said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory, and

wherein said processor outputs addresses from said first terminal to said first memory while at the same time outputting addresses from said second terminal to said second memory.

11. (new) A processor according to claim 10, wherein said first memory outputs graphics data based on said first clock signal.

12. (new) A processor according to claim 10, wherein said second memory outputs said graphics data for displaying based on said second clock signal.

13. (new) A processor according to claim 10, wherein said processor which reads graphics data from said first memory, generates new graphics data from said read graphics data, and writes said new graphics data to said second memory.

14. (new) A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, a second memory which stores graphics data and which is separate from said first memory, said processor comprising:

a first terminal; and

a second terminal for outputting addresses,

wherein said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory, and

wherein said processor outputs addresses from said second terminal to said second memory while at the same time outputting addresses from said first terminal to said first memory.

15. (new) A processor according to claim 14, wherein said first memory outputs graphics data based on said first clock signal.

16. (new) A processor according to claim 14, wherein said second memory outputs graphics data based on said second clock signal.

17. (new) A processor according to claim 14, wherein said processor which reads graphics data from said first memory, generates new graphics data from said read graphics data, and writes said new graphics data to said second memory.

18. (new) A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data and which is separate from said first memory, said processor comprising:

a first terminal; and

a second terminal for outputting/inputting data,

wherein said processor reads graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory,

wherein a transfer amount of data input according to said address output from said first terminal differs from a transfer amount of data output according to said address output from said second terminal, and

wherein said addresses are output from said first and second terminals to said first and second memories respectively at the same time.

19. (new) A processor according to claim 18, wherein said first memory outputs said graphics data based on said first clock signal.

20. (new) A processor according to claim 18, wherein said second memory outputs said graphics data based on said second clock signal.

21. (new) A processor according to claim 18, wherein said processor which reads graphics data from said first memory, generates new graphics data from said read graphics data, and writes said new graphics data to said second memory.